

# Interlaken Interoperability Recommendations

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11 October 2011

Revision 1.6

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## Revision History

<b>Revision 1.6</b> <b>Revision Date: 11 October 2011</b>
<ul style="list-style-type: none"><li>• Added 120G target applications</li><li>• Added 16L Lmax-xoff entry in Table 1</li><li>• Added skew budget sections 3.5-3.7</li></ul>
<b>Revision 1.5</b> <b>Revision Date: 8 December 2010</b>
<ul style="list-style-type: none"><li>• Added retransmission information to section 2.1 and 2.2.</li></ul>
<b>Revision 1.4</b> <b>Revision Date: 04 June 2010</b>
<ul style="list-style-type: none"><li>• Added Section 3.3.1, Board Height Requirements on page 18</li></ul>
<b>Revision 1.3</b> <b>Revision Date: 05 January 2009</b>
<ul style="list-style-type: none"><li>• Added 10.3125 Gb/s SerDes rate options</li><li>• Added references to OIF's electrical specifications</li><li>• Added legal disclaimer page</li></ul>
<b>Revision 1.2</b> <b>Revision Date: 10 September 2008</b>
<ul style="list-style-type: none"><li>• Added section to define Lmax-xoff.</li></ul>
<b>Revision 1.1</b> <b>Revision Date: 11 June 2008</b>
<ul style="list-style-type: none"><li>• Changed naming from "40G", "20G" interfaces to "50G", "25G" interfaces. The "50G" interface has exactly half the throughput of a "100G" interface.</li><li>• Figure added showing interoperability with 10G narrow and 10G wide interfaces</li><li>• Added Physical Interop Recommendations section</li></ul>
<b>Revision 1.0</b> <b>Revision Date: 31 October 2007</b>
<ul style="list-style-type: none"><li>• First release.</li></ul>

# 1 Overview

The Interlaken protocol specification addresses a wide range of chip-to-chip packet transfer needs. It is scalable in bandwidth and has options to optimize the interface towards specific requirements as, for example, low latency burst transfers, unidirectional transfers, etc.

In order to facilitate interoperability between devices from different vendors, the Interlaken Alliance has defined a set of recommended baseline configurations. These recommendations target typical applications at data transfer rates of 10 Gb/s, 25 Gb/s, 50 Gb/s and 100 Gb/s.

Physical interoperability recommendations are also included to facilitate interoperability between reference boards and hardware platforms.

## 2 Logical Interoperability Recommendations

### 2.1 Definitions of Interoperability Parameters

The parameters specified in the next sections are defined in the table below.

Property	Definition	Comments
Number of lanes	One lane means one differential transmit signal pair and one differential receive pair.	
Lane bit rate	Transceiver bit rate. All transceivers in a logical interface are frequency-locked and run at the same bit rate.	10.3125 Gb/s, 6.25 Gb/s and 3.125 Gb/s were selected to match common industry rates.
Backpressure method	Method to signal flow control on a specific logical channel or for the interface link as a whole.	Backpressure signals can either use separate pins, out of band, or be carried in bits in the data path control word, in band.
Packet transfer method	Packets can either be transferred one full packet at a time or as segments, where partial packets on different channels are interleaved.	The two modes are called packet mode and segment mode.
Stop boundary	Where a packet transfer stops as a response to backpressure.	Transmission can either stop at packet boundary, which require larger buffers, or stop at any burst control word within a packet.
BurstMax / BurstMin / BurstShort	<i>BurstMax</i> – maximum size of a data burst <i>BurstMin</i> – smallest size of an end-of-packet burst <i>BurstShort</i> – minimum interval between burst control words	
MetaFrameLength	The quantity of data sent on each lane including one Synchronization Word, one Scrambler State Word, one Diagnostic Word, one or more Skip Words, and the data payload	
Multiple use field	Field is part of the burst control word as defined in the Interlaken protocol specification.	Typical use of this field is to extend the channel ID field or to extend the flow control field.
Rate matching	Granularity of interface rate shaper.	This shaper prevents the transmitter from overflowing the receiver.
Retransmission	Interlaken supports an optional retransmission extension which allows bit errors to be corrected by retransmitting data.	
Comments	Additional comments and observations outside the interoperability recommendation.	

## 2.2 Recommendations for All Transfer Rates

Property	Recommendation
Backpressure method	In-band
Channel count	Not specified, application dependent
Packet transfer method	Not specified, application dependent
Packet Mode Stop Boundary	For link level backpressure: Burst end For channel backpressure: Packet end
Burst Mode Stop Boundary	Burst
BurstMax / BurstMin / BurstShort	256 bytes / 64 bytes / 32 bytes
MetaFrameLength	2,048 words
Multiple use field	Not used
Rate matching	Yes, 1 Gb/s steps
Status Messaging	Not required
Retransmission	Optional, default is disabled
Comments	For unidirectional data paths, out-of-band backpressure may be useful. LVCMOS electrical levels are then preferred.

## 2.3 10 Gb/s Packet Transfers

### 2.3.1 Target Applications

The recommendations were created to provide sufficient performance for typical implementations of these applications:

Application	Frame Sizes
1 port 10 Gigabit Ethernet	64 bytes and up
12 ports Gigabit Ethernet	64 bytes and up
OC192 / STM64 POS framer	40 bytes and up

### 2.3.2 Recommendations

There are two different recommendations at the 10 Gb/s transfer rate to take advantage of widely used serial transceiver rates. For interoperability, an implementation would need to specify if it adheres to the narrow or wide interface option.

### 2.3.2.1 Recommendation #1 – Narrow Interface Option

Property	Recommendation
Number of lanes	3
Lane bit rate	6.25 Gb/s
Electrical Specification	CEI-6G-SR
Comments	10 GE can be optimized into just 2 lanes

### 2.3.2.2 Recommendation #2 – Wide Interface Option

Property	Recommendation
Number of lanes	5
Lane bit rate	3.125 Gb/s

## 2.4 25 Gb/s Packet Transfers

### 2.4.1 Target Applications

The recommendations were created to provide sufficient performance for typical implementations of these applications:

Application	Frame Sizes
2 ports 10 Gigabit Ethernet	64 bytes and up
25 ports Gigabit Ethernet	64 bytes and up
2x OC192 POS framer	40 bytes and up

### 2.4.2 Recommendations

Property	Recommendation
Number of lanes	5
Lane bit rate	6.25 Gb/s
Electrical Specification	CEI-6G-SR

## 2.5 50 Gb/s Packet Transfers

### 2.5.1 Target Applications

The recommendations were created to provide sufficient performance for typical implementations of these applications:

Application	Frame Sizes
5 ports 10 Gigabit Ethernet	64 bytes and up
50 ports Gigabit Ethernet	64 bytes and up
OC768 / STM256 POS framer	40 bytes and up
4x OC192 POS framer	40 bytes and up

### 2.5.2 Recommendations

There are two different recommendations at the 50 Gb/s transfer rate to take advantage of widely used serial transceiver rates. For interoperability, an implementation would need to specify if it adheres to the narrow or wide interface option.

#### 2.5.2.1 Recommendation #1 – Wide Interface Option

Property	Recommendation
Number of lanes	10
Lane bit rate	6.25 Gb/s
Electrical Specification	CEI-6G-SR

#### 2.5.2.2 Recommendation #2 – Narrow Interface Option

Property	Recommendation
Number of lanes	6
Lane bit rate	10.3125 Gb/s
Electrical Specification	CEI-11G-SR
Comment	It is recommended to allow double the skew tolerance (214 UI) for this rate

## 2.6 100 Gb/s Packet Transfers

### 2.6.1 Target Applications

The recommendations were created to provide sufficient performance for typical implementations of these applications:

Application	Frame Sizes
10 ports 10 Gigabit Ethernet	64 bytes and up
100 ports Gigabit Ethernet	64 bytes and up
2x OC768 POS framer	40 bytes and up
8x OC192 POS framer	40 bytes and up

### 2.6.2 Recommendations

There are two different recommendations at the 100 Gb/s transfer rate to take advantage of widely used serial transceiver rates. For interoperability, an implementation would need to specify if it adheres to the narrow or wide interface option.

#### 2.6.2.1 Recommendation #1 – Wide Interface Option

Property	Recommendation
Number of lanes	20
Lane bit rate	6.25 Gb/s
Electrical Specification	CEI-6G-SR

#### 2.6.2.2 Recommendation #2 – Narrow Interface Option

Property	Recommendation
Number of lanes	12
Lane bit rate	10.3125 Gb/s
Electrical Specification	CEI-11G-SR
Comment	It is recommended to allow double the skew tolerance (214 UI) for this rate

## 2.7 120 Gb/s Packet Transfers

### 2.7.1 Target Applications

The recommendations were created to provide sufficient performance for typical implementations of these applications:

Application	Frame Sizes
12 ports 10 Gigabit Ethernet	64 bytes and up
3 ports 40 Gigabit Ethernet	64 bytes and up
OTU4 or 3x OTU3/OTU3e	40 bytes and up
3x OC-768 POS Framer	40 bytes and up
12x OC-192 POS Framer	40 bytes and up

### 2.7.2 Recommendations

Property	Recommendation
Number of lanes	16
Lane bit rate	10.3125 Gb/s
Electrical Specification	CEI-11G-SR
Comment	It is recommended to allow double the skew tolerance (214 UI) for this rate

## 2.8 Summary of Lane Recommendations

Transfer Rate	Recommendation #1 Wide Options			Recommendation #2 Narrow Options		
	Lanes	Rate [Gb/s]	Electrical	Lanes	Rate [Gb/s]	Electrical
10 Gb/s	5	3.125		3	6.25	CEI-6G-SR
25 Gb/s	5	6.25	CEI-6G-SR			
50 Gb/s	10	6.25	CEI-6G-SR	6	10.3125	CEI-11G-SR
100 Gb/s	20	6.25	CEI-6G-SR	12	10.3125	CEI-11G-SR
120 Gb/s				16	10.3125	CEI-11G-SR

## 2.9 Multirate Interoperability

The per-rate recommendations are for interoperability between components of the same capacity; e.g. a 50 Gb/s framer connected to a 50 Gb/s packet processor. Additionally, there is also a possibility to interoperate with multiple lower-capacity components if the lower speed recommendations are also implemented.

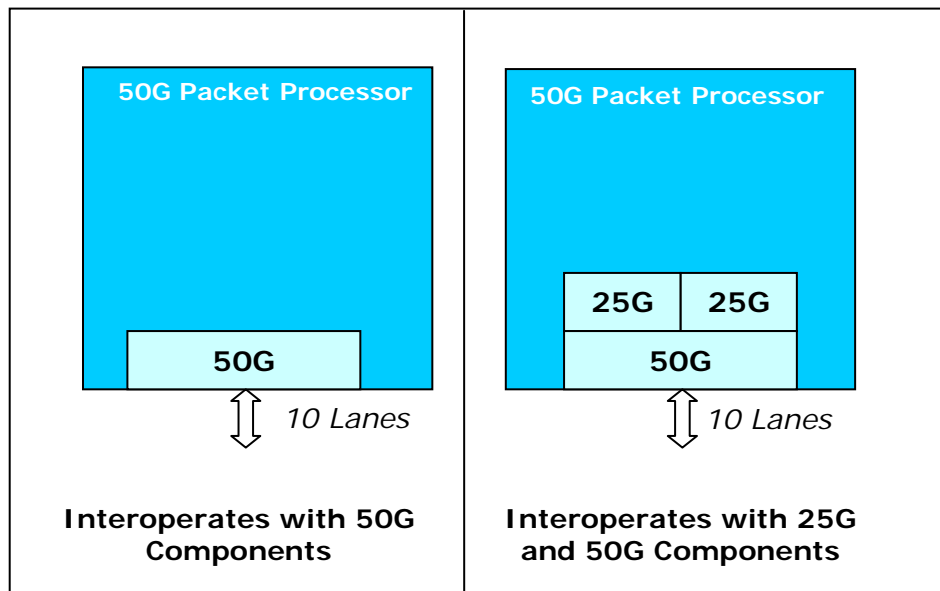
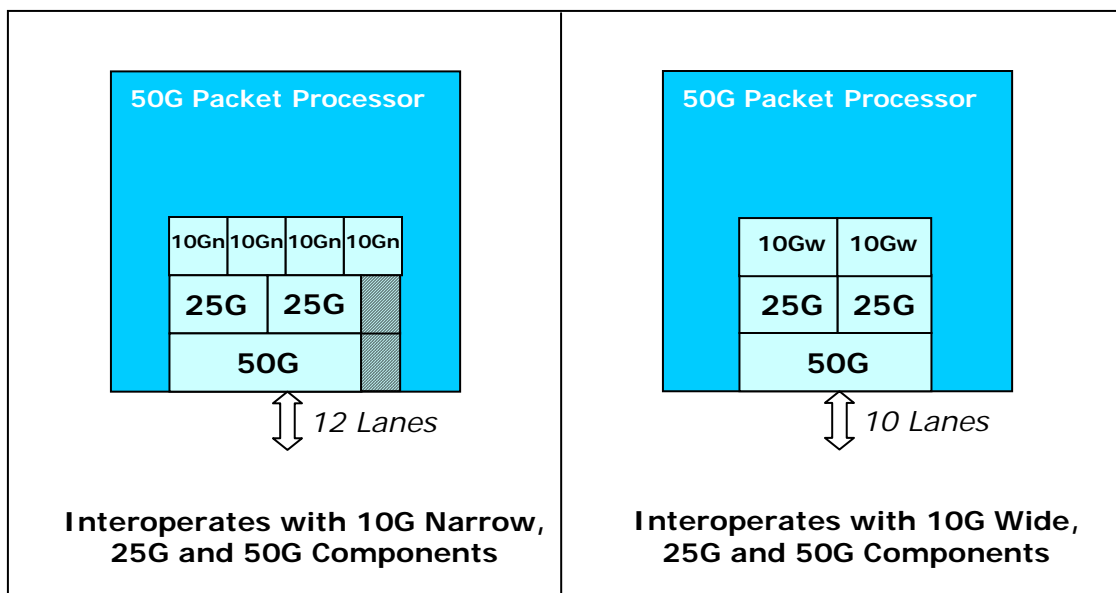


Figure 1: Example of Interoperability with Lower Capacity Components

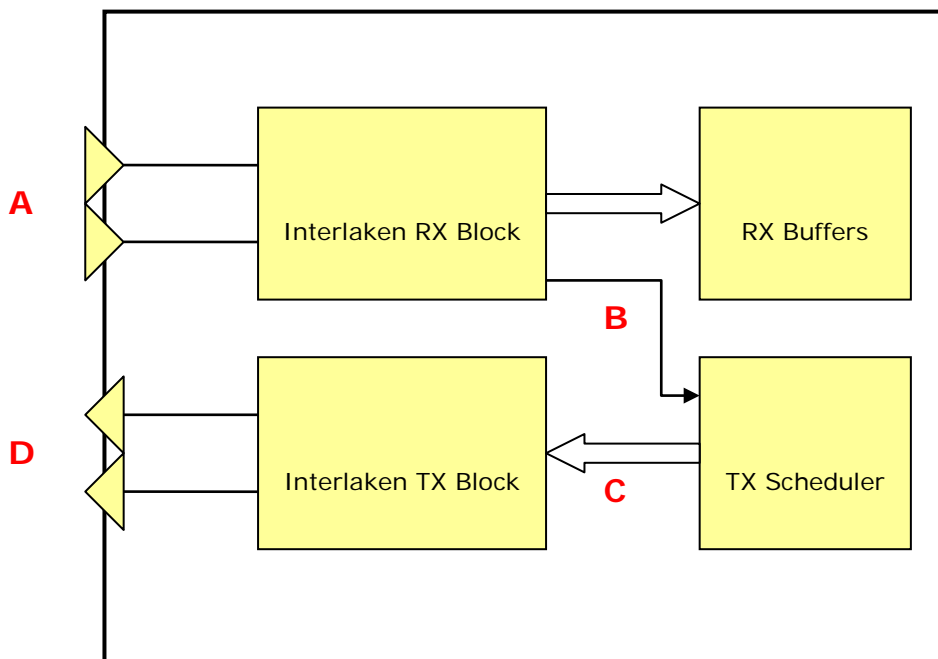


**Figure 2: Example of Interoperability with 10G Components**

## 2.10 Latency Requirements

In order to improve interoperability and to avoid over-design of buffers in a receiving device, the interoperability guideline defines the maximum time a transmitting device should respond after it receives XOFF information. This parameter is termed  $L_{max-xoff}$  and is defined as the maximum number of bytes the transmitter is allowed to transmit after XOFF information appears at the input pins of the transmitting device.

Figure 3 shows a high level block diagram of a typical transmitter. The transmitter must ensure no more than  $L_{max-xoff}$  bytes go through point D after XOFF is seen at point A. The various contributors to  $L_{max-xoff}$  include the delay through the Interlaken RX block (point A->B), the time it takes for the TX Scheduler to stop transmitting data (point B->C), and how much data is already in flight through the Interlaken TX block (point C->D).



**Figure 3 Transmitter Block Diagram**

Table 1 defines  $L_{max-xoff}$  for different interface configurations. The numbers apply to burst mode operation. For packet mode, one MTU must be added to the  $L_{max-xoff}$  values. Additionally, the numbers are based on in-band flow control, since out-of-band flow control is typically faster and so the numbers would be less.

The numbers are independent from the number of channels, though valid for a small number of channels.

Number of Lanes	Serial Rate	$L_{max-xoff}$
	(Gb/s)	(Bytes)
5	3.125	1,536

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3	6.25	1,280
5	6.25	1,792
6	10.3125	6,400
10	6.25	6,400
12	10.3125	12,484
16	10.3125	16,645
20	6.25	12,484

**Table 1 Lmax-xoff Definitions**

## 3 Physical Interoperability Recommendations

In order to facilitate the physical interoperability between devices, the Interlaken Alliance has defined a set of recommended connector types, connector pin assignment, and connector board placements.

### 3.1 Connector Type

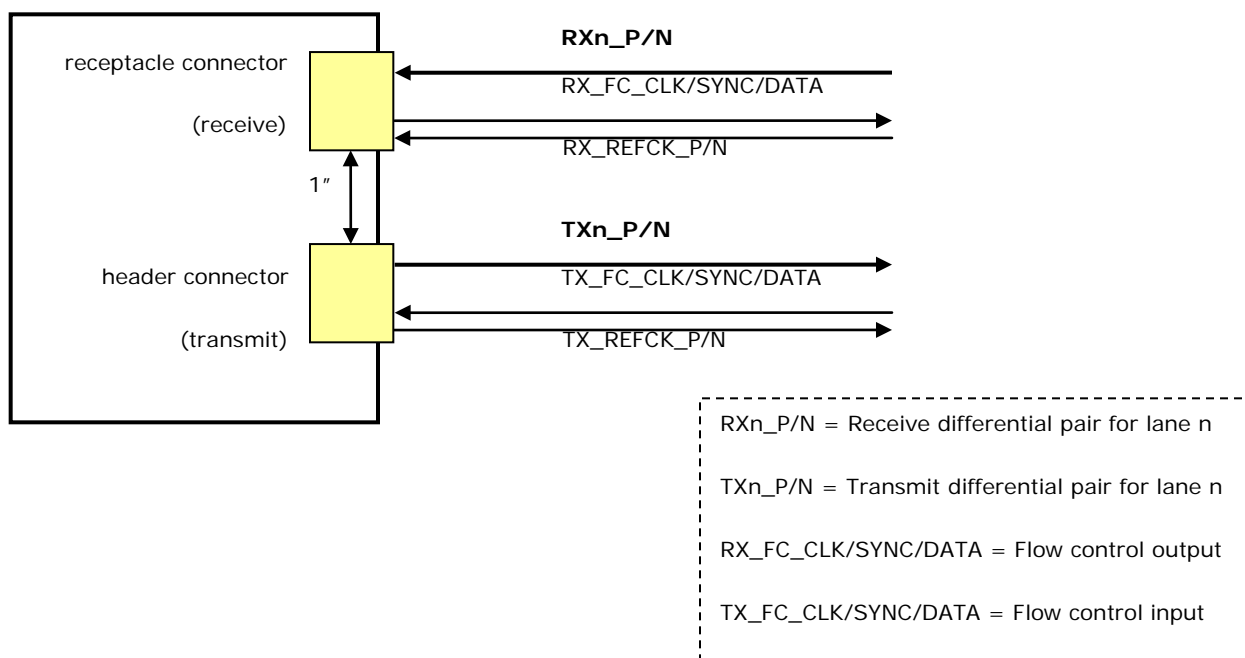
The recommended common connector is FCI AirMax VS<sup>®</sup> High Speed 4-Pair 120-pos 3-mm 10 IMLA Right Angle Header / Receptacle connectors for coplanar connections.

The part numbers for the connectors are 10035515 (header) and 10045722 (receptacle).

The header connector transmits data across the interface while the receptacle connector receives data from the interface.

### 3.2 Connector Pin Assignment

A common pin assignment for the connectors is shown in the following diagrams. Figure 4 below shows the signal names used in the pin assignment. Figure 5 below shows the pin assignment of the differential pairs for the receiver. Since the pin labeling of the header and receptacle connectors are mirror image of each other, the transmit and receive differential pairs have the same pin assignment (e.g. TX0\_P at A7 of header will mate with RX0\_P at A7 of receptacle).



**Figure 4: Signal Names for Connector Pin Assignment**

	10	9	8	7	6	5	4	3	2	1
<b>A</b>	GND	<b>RX3_P</b>	GND	<b>RX0_P</b>	GND	<b>RX7_P</b>	GND	<b>RX4_P</b>	GND	<b>RX_REFCK_P</b>
<b>B</b>	GND	<b>RX3_N</b>	GND	<b>RX0_N</b>	GND	<b>RX7_N</b>	GND	<b>RX4_N</b>	GND	<b>RX_REFCK_N</b>
<b>C</b>	GND	GND	GND	GND	GND	GND	GND	GND	GND	<b>GND</b>
<b>D</b>	GND	GND	<b>RX2_P</b>	GND	<b>RX1_P</b>	GND	<b>RX6_P</b>	GND	<b>RX5_P</b>	<b>GND</b>
<b>E</b>	<b>RX_FC_CK</b>	GND	<b>RX2_N</b>	GND	<b>RX1_N</b>	GND	<b>RX6_N</b>	GND	<b>RX5_N</b>	<b>GND</b>
<b>F</b>	GND	GND	GND	GND	GND	GND	GND	GND	GND	<b>GND</b>
<b>G</b>	GND	GND	GND	GND	GND	<b>RX8_P</b>	GND	<b>RX9_P</b>	GND	<b>RX11_P</b>
<b>H</b>	GND	<b>RX_FC_SYNC</b>	GND	<b>RX_FC_DATA</b>	GND	<b>RX8_N</b>	GND	<b>RX9_N</b>	GND	<b>RX11_N</b>
<b>I</b>	GND	GND	GND	GND	GND	GND	GND	GND	GND	<b>GND</b>
<b>J</b>	<b>RX13_P</b>	GND	<b>RX15_P</b>	GND	<b>RX12_P</b>	GND	<b>RX10_P</b>	GND	<b>RX14_P</b>	<b>GND</b>
<b>K</b>	<b>RX13_N</b>	GND	<b>RX15_N</b>	GND	<b>RX12_N</b>	GND	<b>RX10_N</b>	GND	<b>RX14_N</b>	<b>GND</b>
<b>L</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>	<b>GND</b>

**Figure 5: Connector Pin Assignment for Differential Pairs (receiver shown)**

The lanes needed to support a certain data transfer rate shall occupy the lower-numbered differential pairs (e.g. 25 Gb/s interface shall use RX0\_P/N through RX4\_P/N).

The upper-numbered pairs are treated as spare pins for user-defined purposes. If unused, these pins shall be left unconnected.

The flow control signals (FC\_CK, FC\_SYNC and FC\_DATA) are used only when out-of-band backpressure is supported. If unused, these pins shall be left unconnected.

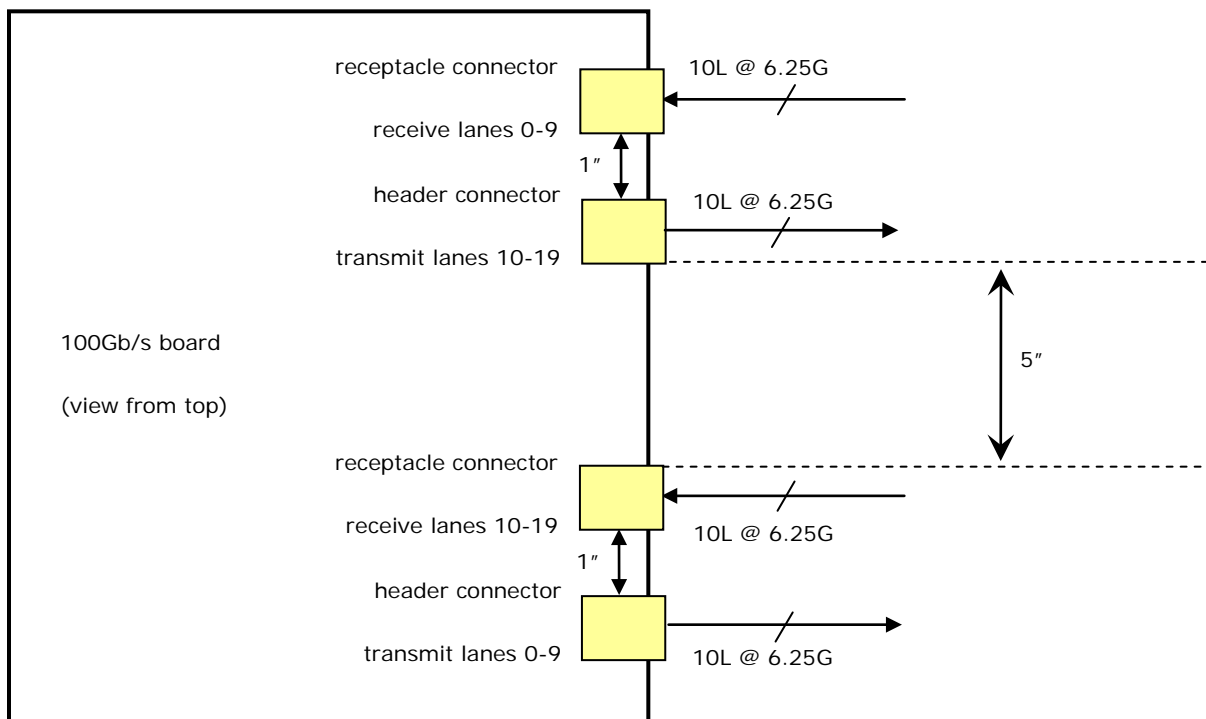
The REFCK\_P/N pair can be optionally used to pass a reference clock across the interface. If unused, these pins shall be left unconnected.

The 100 Gb/s interface shall employ 2 sets of connectors with the same pin assignment for 50 Gb/s interface. The placement of these connectors is described in Section 3.3 below.

### 3.3 Connector Placement

For all interface rates, the header and receptacle connectors shall be placed 1" apart (1155 mil between pins A10 of 2 connectors) as shown in Figure 6 below. When viewed from the top with the connectors along the right edge of the board, the header shall be placed below the receptacle.

For 100 Gb/s interface, two sets of connectors are needed. The two connectors shall be placed 5" apart as shown below. For 100 Gb/s interface to interoperate with 50 Gb/s (or lower) interface, channel mapping will be needed on the 100 Gb/s interface, as shown in Section 3.4.8 on page 22.



**Figure 6: Connector Placement for 100 Gb/s Interface**

### 3.3.1 Board Height Requirements

For ease of interoperability testing, a standard board height of 1.37 inches to the top of the board is recommended as shown in Figure 7 below.

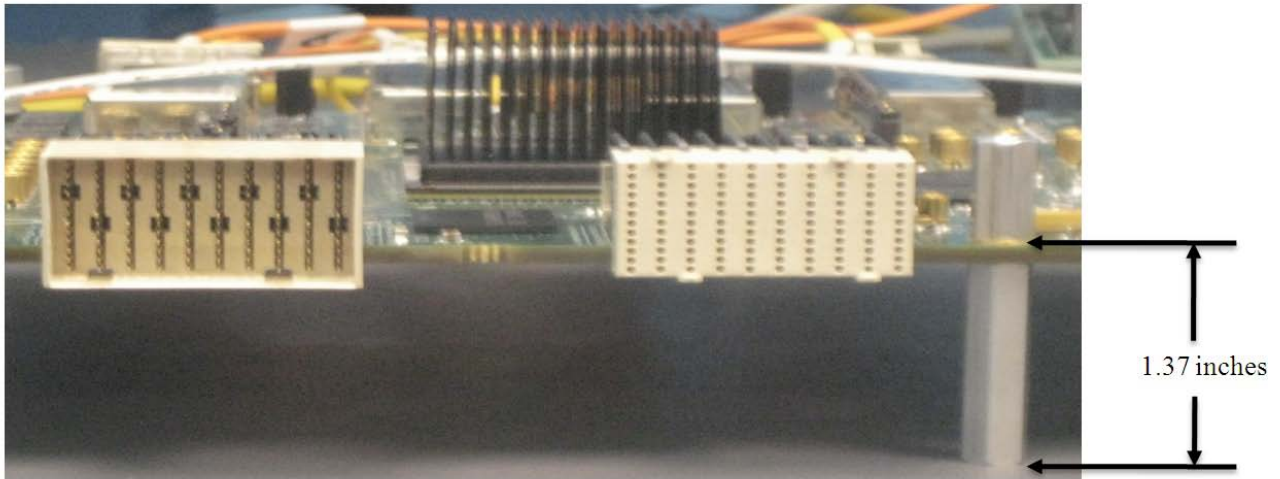
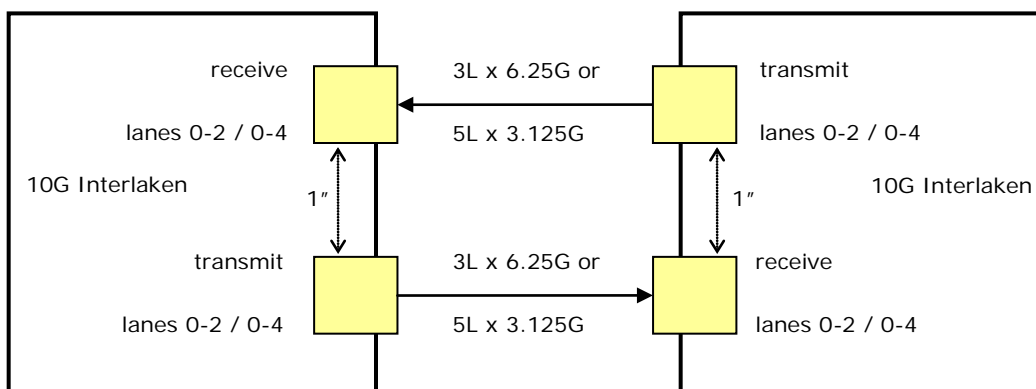


Figure 7: Standard Interlaken Board Height

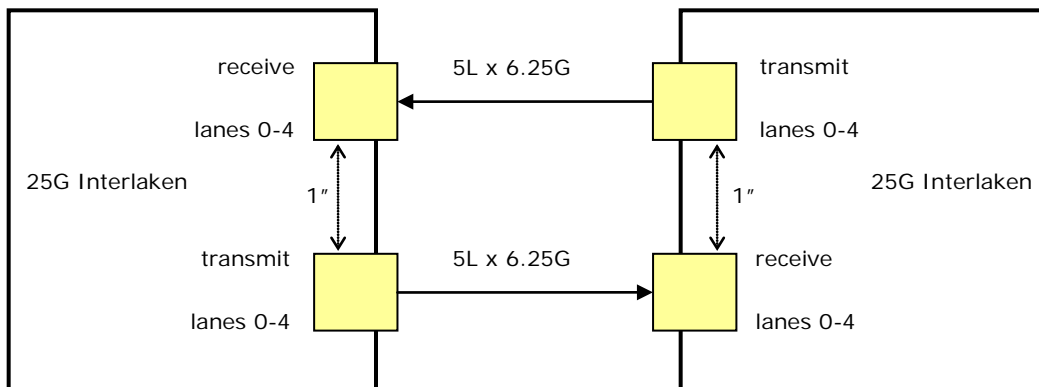
## 3.4 Physical Interoperability Examples

The following sections show examples of how two evaluation boards can be connected together based on the recommendations above.

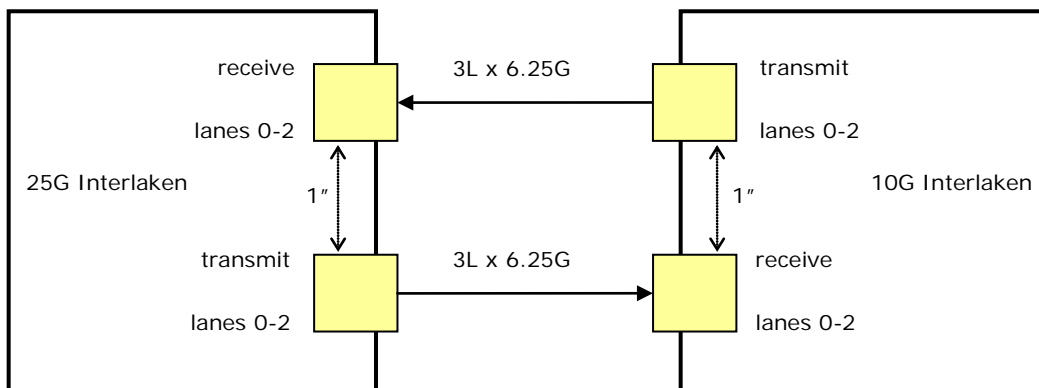
### 3.4.1 Connecting 10 Gb/s to 10 Gb/s



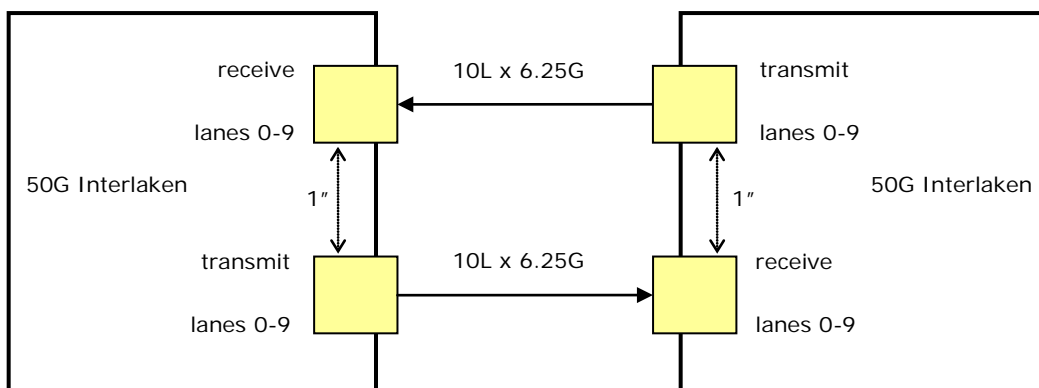
### 3.4.2 Connecting 25 Gb/s to 25 Gb/s



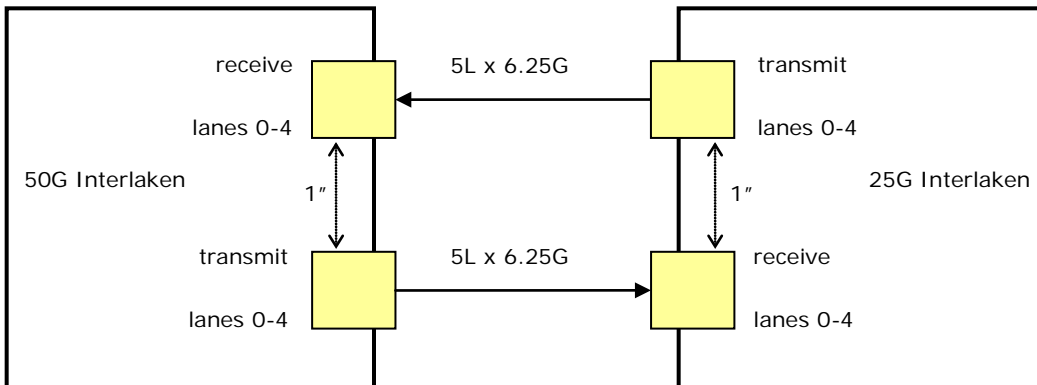
### 3.4.3 Connecting 25 Gb/s to 10 Gb/s



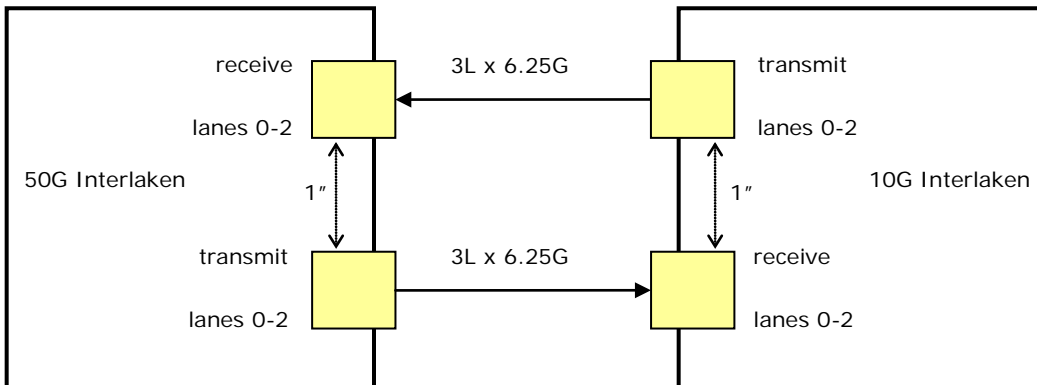
### 3.4.4 Connecting 50 Gb/s to 50 Gb/s



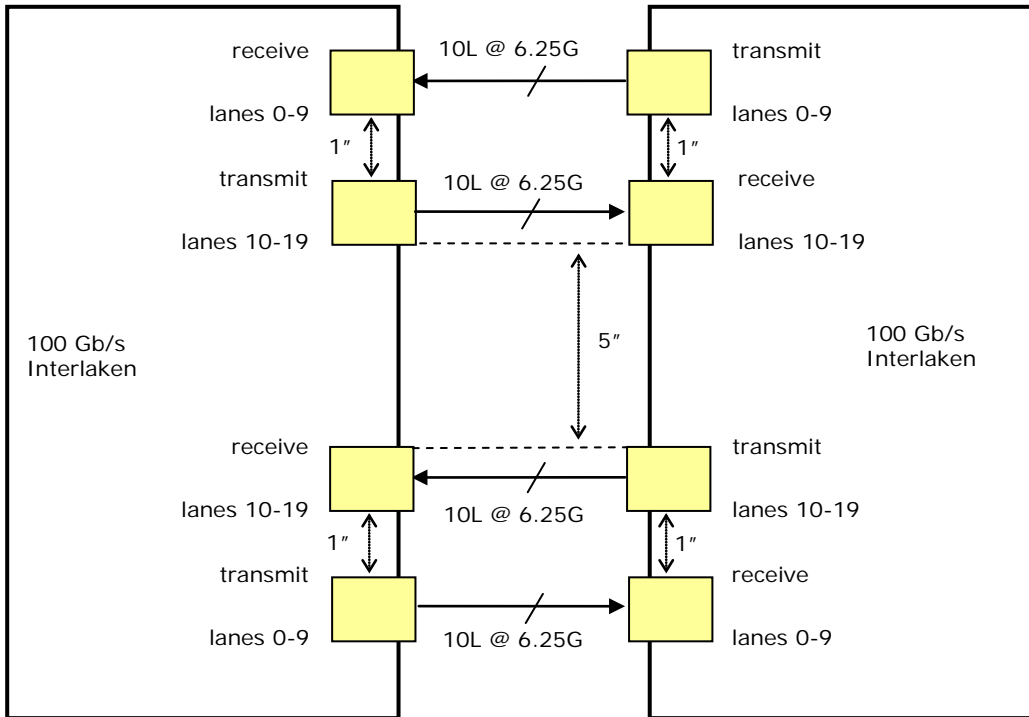
### 3.4.5 Connecting 50 Gb/s to 25 Gb/s



### 3.4.6 Connecting 50 Gb/s to 10 Gb/s



### 3.4.7 Connecting 100 Gb/s to 100 Gb/s

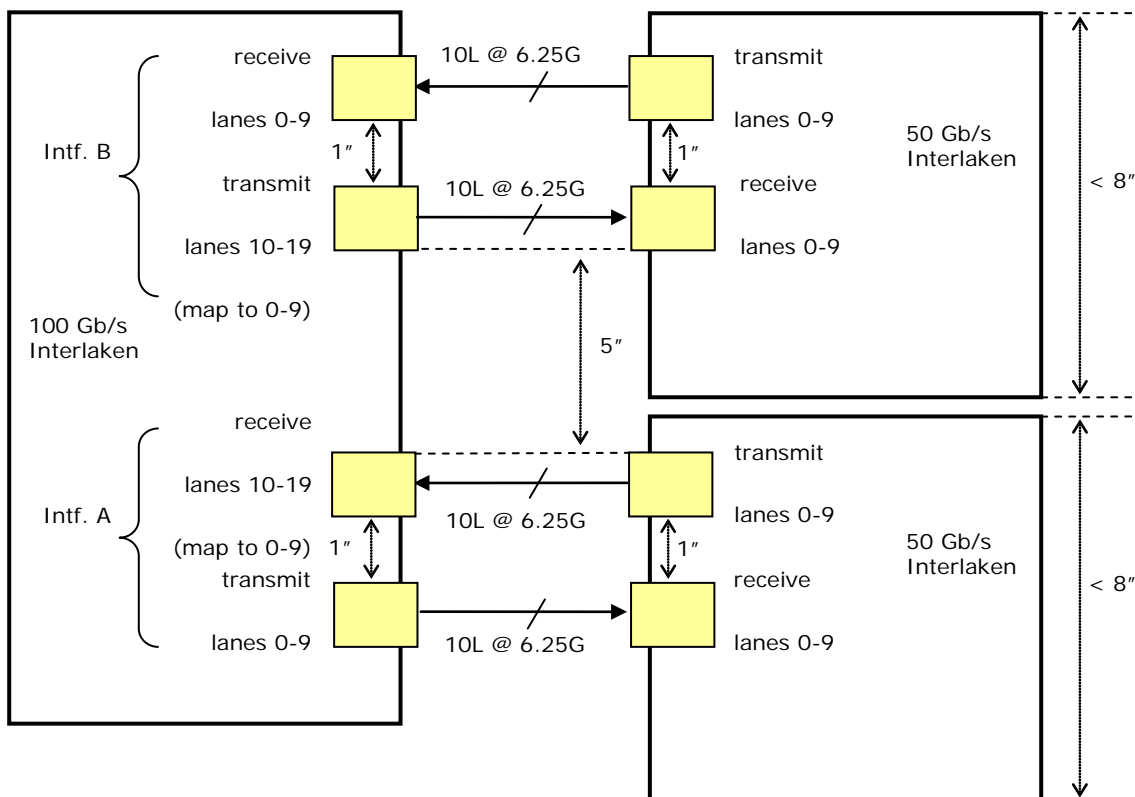


### 3.4.8 Connecting 100 Gb/s to 50 Gb/s

For 100 Gb/s to interop with lower rate interfaces, channel mapping is required as shown below:

- Map RX lanes 10-19 to RX lanes 0-9 of Interlaken Interface A
- Map TX lanes 10-19 to TX lanes 0-9 of Interlaken Interface B

Also, for connecting 2 evaluations boards of lower interface rate, there should be sufficient space for the boards to be connected side-by-side. Each board should not be more than 8" wide.



### 3.4.9 Connecting to Multiple Interlaken Interfaces

As shown in Section 2.8, interoperability with multiple lower-capacity components is also possible. This section describes the general recommendations of how this can be achieved. However, not all combinations can be covered by these recommendations. As such, for more complex interoperability cases, they will serve only as a set of guidelines.

#### 3.4.9.1 Lanes Assignment

For connection between a higher-capacity component with multiple lower-capacity components (e.g. 50 Gbps component connecting to two 25 Gbps components), these recommendations apply:

- Components supporting multiple Interlaken interfaces of rates of 50 Gbps and lower should use consecutive lanes starting with lane 0 in the following order:
  1. for all 50G interfaces (if any)
  2. for all 25G interfaces (if any)
  3. for all 10G-wide interfaces (if any)

4. for all 10G-narrow interfaces (if any)

These lanes should use only 1 set of connectors. If necessary, the spare lanes can be used, giving a maximum of 16 lanes per connector.

For example, a 50G component that also supports interoperability with four 10G-narrow components, uses 12 lanes (lanes 0-2, 3-5, 6-8 and 9-11) all from the same set of connectors. In this case, spare lanes 10 and 11 are used.

- Components supporting 100 Gbps shall use 2 sets of connectors as shown in Figure 5 above. Each set of connectors should be treated as a separate interface, connecting to a single component, or connecting to multiple lower-rate components.

For example, a 100G component that also supports 2 x 25G interfaces can either route each 25G interface to lanes 0-4 of each of the 2 connector sets, or route both interfaces to 1 connector set, using lanes 0-4 and 5-9.

- Lane mapping should be used to support multirate interoperability.
- Since in-band flow control is part of the interoperability recommendations for all rates, out-of-band flow control need not be supported.
- For any cases where extra lanes are required, the spare lanes should be used.

### 3.4.9.2 More Multirate Interoperability Examples

- 50G connecting to 2 x 25G: lanes 0-4 connect to one 25G component while lanes 5-9 connect to the other.
- 50G connecting to 4 x 10G-narrow: lanes 0-2, 3-5, 6-8, 9-11 connect to each of the 10G-narrow components. In this example, lanes 10 and 11 are spare lanes.
- 50G connecting to 1 x 25G and 2 x 10G-narrow: lanes 0-4 connect to the 25G component, while lanes 5-7, 8-10 connect to each of the 10G-narrow components. Lane 10 is a spare lane.
- 100G connecting to 2 x 50G: this is shown in Section 3.4.8 on page 22.
- 100G connecting to 4 x 10G-narrow: lanes 0-2, 3-5, 6-8, 9-11 (from one set of connectors) connect to each of the 10G-narrow components. Lanes 10 and 11 are spare lanes. Alternatively, 4 x 10G-narrow components can use 2 sets of connectors. Two of the 10G-narrow interfaces can go through 1 set of connectors using lanes 0-2 and 3-5, while the other two 10G-narrow interfaces go to the 2nd set of connectors.

## 3.5 PCB Intra-Lane Skew Budget

Skew between P/N signals in each differential pair must be managed for each transmit and receive lane and include compensation for skew within the connector. Maximum skew between P/N shall be 3ps after subtracting connector delay compensation shown in the table below from the P lane (e.g. If RX0\_P is 710ps then RX0\_N should be 700ps +/-3ps or 697 to 703 ps). The connector skew compensation should be located as close to the connector as possible.

<b>Lane</b>	<b>Delay(ps)</b>
<b>0, 3, 4, 7</b>	10
<b>1, 2, 5, 6</b>	2.5
<b>8, 9, 11</b>	8
<b>10, 12, 13, 14, 15</b>	7.5

### 3.6 AC Coupling

Each Lane connected to the receive receptacle connector should include AC coupling capacitors on each lane using a value of 100nF.

### 3.7 Signal Integrity Considerations

Lanes 0, 3, 4 and 7 have higher insertion loss through the connector. For interface rates higher than 6.5 Gb/s these lanes should be closely examined to minimize any additional PCB losses. Suggested layout options include:

- Backdrill these lanes at the connector and use the lowest available routing layer at the connector via to minimize via stubs
- Include an outer GND via for the P signal to reference on row As